Patent Claims

1. Method for the management of data received via a data bus, the data being transmitted in bus packets having a variable length, the data being divided into data blocks (DB0-DB7) having a defined length, a combination of a defined number n of data blocks (DB0-DB7) forming a data source packet (SP0-SP2), section-by-section transmission of the data source packet (SP0-SP2) within the framework of data blocks being permitted, **characterized in that** modulo-n counting of the data blocks (DB0-DB7) is carried out in order to determine the data source packet boundaries, and in that the beginning of a new data source packet (SP1, SP2) is signalled to a memory management device (31) at the beginning of the next counting interval.

2. Method according to Claim 1, in which each bus packet is subjected to CRC checking and the checking results are buffer-stored in order to be able to ascertain whether a data source packet (SP0-SP2) transmitted in two or more bus packets has been transmitted without any errors.

3. Method according to Claim 1 or 2, in which a reference counter reading is transmitted in each bus packet in order to check the completeness of the transmitted data, and in which comparison counting of the received data blocks (DB0-DB7) is effected and, when the data block associated with the reference counter reading is received, the result of the comparison counting is compared with the reference counter reading and an error signal (DBC_ERR) is output in the event of non-correspondence.

4. Method according to one of the preceding claims, in which the defined number n of data blocks (DB0-DB7) of a data source packet (SP0-SP2) corresponds to the number

8 and the modulo-n counting is correspondingly modulo-8 counting.

5. Apparatus for carrying out the method according to one of the preceding claims, having a memory unit (30) to which the received data are written in order, and having a memory management device (31), **characterized in that** a modulo-n counter (33) is provided, which counts the received data blocks (DB0-DB7) and outputs a data source packet start signal (SP_ST) to the memory management device (31) at the beginning of the next counting interval.

6. Apparatus according to Claim 5, which furthermore has a CRC checking unit (32), by means of which the data in the received bus packets are checked with regard to freedom from errors, where the checking results of a plurality of successive bus packets are buffer-stored and combined if the data source packet start signal (SP_ST) has been identified, and where the CRC checking unit (32) outputs an error signal (CRC_ERR) if one of the combined checking results includes an identified error.

7. Apparatus according to Claim 5 or 6, which furthermore has a data block reference counter (34), which effects the comparison counting of the received data blocks (DB0-DB7), and where comparison means are provided which compare the counter reading of the data block reference counter (34) with the received reference counter reading of the bus packet and output an error signal (DBC_ERR) in the event of non-correspondence.

8. Apparatus according to one of the preceding claims, which furthermore has a data counter (35), by which the data are counted in particular in units of bytes and which outputs a data block counting signal if the number of data that have been counted are as many as are defined as belonging to a data block (DB0-DB7).

9. Apparatus according to one of the preceding claims, where the data bus is designed according to the IEEE 1394 standard and the apparatus is part of a data link layer module in the interface for this data bus.